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Implementation of Embedded Real-time Image Processing System based on ARM and DSP

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ABSTRACT: With the rapid development of modern information technology, the research and applications of image processing, especially the real-time image processing technology has attracted widespread attention of scholars. At the same time, along with the fast development of network, mobile communication and multimedia technology, embedded system has been more widely used. The development of embedded and DSP technology has promoted the new theories' generation and application of image processing technology. Therefore, how to apply ARM and DSP processor structure to the new method of real-time image processing system has very important theory and application value. This paper, according to the actual demand, introduces the embedded image processing system function and general design method based on ARM and DSP, mainly for hardware design of the system's DSP and ARM. From the performance parameters of the test, it can be concluded that the designed system in this paper achieves cooperative work on the ARM and DSP hardware platform, realizing the data real-time transmission, and it has an important guiding significance for the improvement of image processing system.

KEYWORDS: Image processing; Embedded system; ARM; DSP.

INTRODUCTION

In recent years, with the rapid development of computer technology, microelectronics technology, microprocessor with better performance, smaller volume, lower power consumption has appeared. And ARM (Advanced RISC Machine) is one of the best. Due to the wide range of influence in 32-bit embedded RISC area, it has become the first choice in the field of 32-bit microprocessors [1-5].

With the development of electronic technology, real-time image processing technology is one of hot fields in the word. The traditional method using single processor system already cannot adapt to the requirement of a large number of data processing and calculation, especially in today's popular areas such as electronic countermeasures, high speed image processing, intelligent identification, sonar detection and so on. Therefore, embedded processing system with strong real-time and processing performance, a large amount of data transmission should be adopted [6, 7]. DSP chip is designed for rapid implementation of various digital signal processing algorithms, with special structure microprocessor, and its processing speed is as high as 2000 MIPS, 10 to 50 times faster than CPU. In addition, the new generation of DSP chip internal has integrated HPI (Host Port Interface), conducting data communication with other chips (host computer) easily, through the HPI, the host computer can access to almost all memorizer except Cache of DSP interior [8-11].

ARM and DSP, as the core of the real-time image processing system, has certain disadvantages, at the same time, and also has irreplaceable advantages of opposite side. However, the disadvantage and advantage complement each other and make up for each other.

This paper, combined with the advantages of ARM and DSP, has proposed embedded image processing system based on ARM and DSP, solving the faults of low processing efficiency and low small calculating amount effectively. Meanwhile, it has played a positive role on the realization of engineering application and social significance brought by engineering application in the field of signal processing areas which requiring large computation, complex dispose, strong data throughput.

THE COMPARISON AND SELECTION OF HARDWARE PLATFORM

The software development work of embedded system is closely related to the underlying hardware platform, the first is to be familiar with processor chip features and command structure and others located in the core, the second is to be familiar with the control circuit and peripheral equipment of hardware platform. The system, CPU as the core, is

convenient for man-machine interaction and standard interface equipment communication; DSP is mainly used to develop embedded signal processing system, not emphasizing human-computer interaction and generally not needing a lot of communication interface. As for the embedded application, the distinction between embedded CPU and DSP is that one focus on the control, and the other focus on calculation.

There are many video data needed to be processed in the design, determining that multimedia processor is indispensable unit. According to this basic principle, there are two different architecture schemes of hardware platform: one is the separating unit architecture used by digital signal processing (DSP) chip and CPU control chip; the other is dual-core architecture integrated by signal processor and general processor. This paper adopts two separated units DSP and ARM, so the two independent systems can accomplish the design requirements, and also lay the foundation for subsequent improvement work.

THE COMPOSITION OF DSP PARTIAL HARDWARE PLATFORM

Digital signal processor (DSP), since 1982, has become a necessary achieving tool of embedded high-speed computing platform. With the development of multimedia technology, a new class of DSP devices: media processors, has got more and more attention of the industry. The world's largest DSP maker, Texas instruments (TI) has launched a high-performance media processor TMS320DM642 recently, gaining a wide range of recognition with its excellent performance.

TMS320DM642 processor

TMS320DM642 is a kind of DSP chip facing to multimedia applications launched by TI Company. Based on the improved C6x+kernel and integrate, it further integrates with video/audio interface, Ethernet interface, PCI and so on. The internal uses improved Harvard structure which the data is separate with program bus but not addressing alone, improving the flexibility and data throughput. With multiple processing units, it can operate 8 parallel instructions in the same period at most, improving the running speed greatly. The functional block diagram is shown in Figure 1:

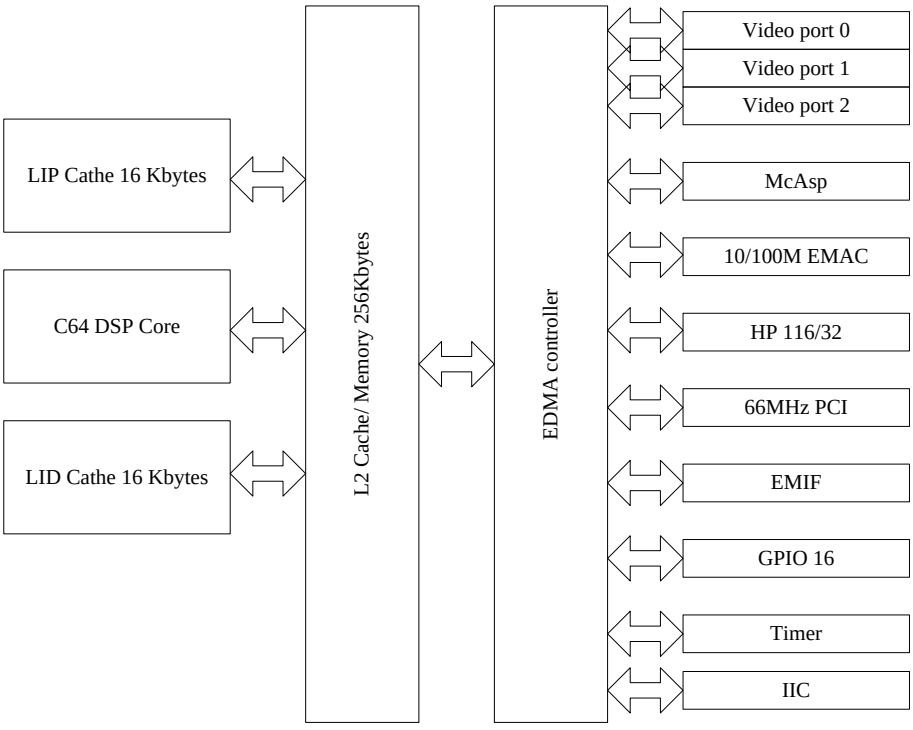

Figure 1. The structure of DM642.

All of the peripherals are connected to the DSP core in DM642 through enhanced DMA controller. The core includes two nearly identical sections, and each section contains a set of general registers (32 * 32-bit) and four functional modules (L, S, M and D) with each functional module performing a kind of operation. Of which the L and S units can perform most logic, arithmetic, displacement and other calculation, M unit mainly performs multiply operation, and D unit mainly performs addressing and some simple arithmetic. Each section also includes a set of data path LD used to

read data, ST used to store data, and address channel DA, in addition, there are cross channels X1 and X2 between the two sections.

The CPU clock frequency of this chip can reach to 600 MHz, there are 8 32-bit function units in CPU interior, operating 8 instructions at the same time, if you can make full use of the eight functional units, under the condition of water completely, and the chip's instruction throughput will reach 48 OOMIPS. The chip internal supports two levels of Cache, of which the first level Cache is not visible to the developer, and the second level Cache size is configurable, the chip automatically complete the maintenance of data consistency between the two levels of Cache. With the support of the two levels of Cache, the executive speed of CPU is accelerated greatly. At the same time, the 64 bit width EMIF can be seamlessly connected to the SDRAM, SRAM and other memorizer, convenient for the expansion of the storage resources.

The composition of DM642 system module

The main parts of hardware platform of DM642 image processing system include SDRAM, video demodulator, audio codec, Ethernet interface, FLASH and watchdog module. The overall structure diagram of system is shown in Figure 2:

SDRAM memorizer. This is the main memorizer of the system, constituting 4 M * 64-bit memorizer with two 4M*32 –bit chips. It connects on EMIF of DM642, using CEO addressing space. In actual operation, most of the programs and data are stored here.

The video demodulation section. Analog video input by camera is converted into digital signals through the module, and transferred to the DSP for processing. It supports analog video formats with PAL system and NTSC system and S terminal video. There are two way video inputs, connecting to VP0 and on VP1 interface of DM642 respectively. The format of output data flow can be BT656 or original Y/C video flow.

Audio codec. Audio codec can perform A/D and D/A transformation, convenient for acquisition and playback of audio. It connects the McASP interface on DSP. This module can be for full-duplex operation, that is to say, the input and output of sound cannot influence each other.

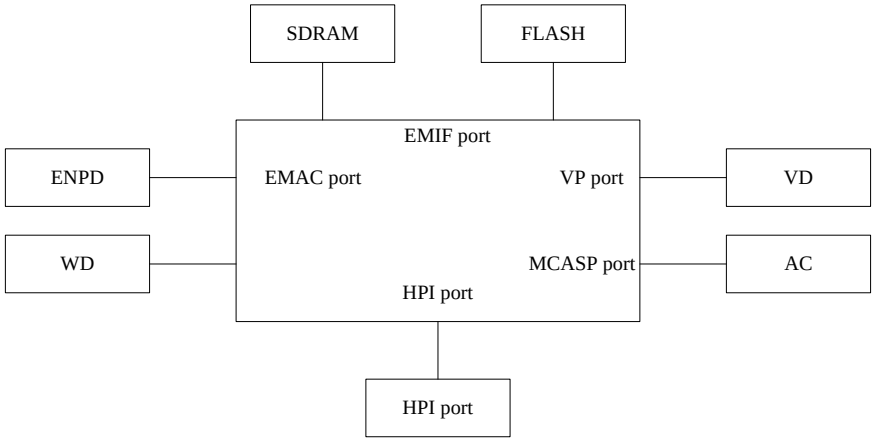

Figure 2. The system diagram of DM642.

FLASH section. The 4M*8 FLASH chip is used as program memory of system, when the system self-starting with power, DSP will read automatically the saved user program, and copy the program to the SDRAM and operate. The FLASH is connected on the EMIF, using CEI address space.

Ethernet interface. DM642 provides an Ethernet interface, Ethernet communication can be realized as long as the external connecting a physical device. DSP internal provides a set of registers, and it can make Ethernet interface receive or send 1024 packets without DSP core intervention. Ethernet interface of DM642 can support 10/100 MHz full-duplex mode, broadcast and multicast. It also can connect multiple external physical layer devices to realize multiple network transmission.

HP interface. Host port interface (HPI) of DM642 provides three registers, making the external master control chip access to address space of the inside of the DSP conveniently. And it is a kind of parallel, data address multiplex trunk,

can be directly connected to the trunks of other control chips after isolator. The host computer can visit addressing space of the whole DSP through HPI, supporting a single mode or burst mode data transmission.

Watchdog and power part. Because the system may be work long hour under the condition of unattended, the systematic stability is also very important. Watchdog circuit provides a mechanism which making the system automatic recovery from the crash, when the effective port of watchdog is not refreshed by the system for a long time, the watchdog circuit will automatically reset the system, making the system away from crash state. The watchdog connects on the GPIO. There is an enable signal on the watchdog chip, and using it watchdog can stop action, making it not affect the debugging of the system

THE COMPOSITION OF ARM HARDWARE PLATFORM

The full name of the ARM is Advanced RISC Machine, and it is a kind of high performance and low power consumption RISC chip. It is designed by the British ARM company, and the company neither produces nor designs chip, but designs efficient IP kernel, authorized for semiconductor company use. Almost all the major semiconductor manufacturers in the world produce general chips based on ARM architecture, or insert the relevant technology of ARM in the special chip. At present, the application fields of the ARM are very wide, accounting for 75% market share of 32-bit RISC microprocessor.

S3C2410 Processor

High-performance processor SOC 53 C2410 produced for mobile terminal by South Korea's Samsung semiconductor company is selected in the design. 53 C2410 is a 16/32- bit RISC microcontroller with low cost, low power consumption, small volume and high performance. The process is mainly for mobile equipment terminals based on ARM920T kernel. At the same time, it also used a novel bus architecture called AMBA (Advanced Microcontroller Bus Architecture). The S3C24lO internal structure is shown in Figure 3.

53C2410 internal integrates with rich on-chip peripherals resource, mainly including:

1)1.8VARM kernel, 3.3V memorizer, 3.3V external I/O, with 16 KB instruction cache/ 16 KB data cache and MMU microprocessor

2) External storage controller (SDRAM control and Chip Selection logic);

3) LCD controller (support to 4K STN and 256K TFT), dedicated DMA of LCD of channel 1;

4) DMA;The DMA with external request of channel 4;

5) UART of channel 3 (IRDA1.0, 16-ByteTxFIFO and 16-ByteRxFIFO)and SPI of channel 2;

6) HC bus controller of channel 1 / IIS bus controller of channel 1;

7) SD host computer interface which is version 1.0, compatible Multi-Media card agreement which is version 2.11;

8)2 USB host computer/1 USB equipment (USB1.1);

9) PWM timer of channel 4 and timer of channel 1 inside;

10) Watchdog circuit;

11)117-bit general 1/0 port, the external interrupt source of channel 24;

12) Power control: regular, slow, idle, and outage mode;

13) 10-bit ADC and touch screen interface of channel 8;

14) Real-time clock (RTC) with calendar Function;

15) On-chip clock generator with phase-locked loop

S3C2410 internal has integrated microprocessor and some commonly used peripheral components, reducing the cost of the whole system greatly and eliminating additional devices of system configuration, and it has provided an efficient hardware platform for embedded system. Because the S3C241O chip internal has integrated with USB1.1 host interface, and the external USB host chip can be removed, thereby saving a lot of work and be able to complete the design task better.

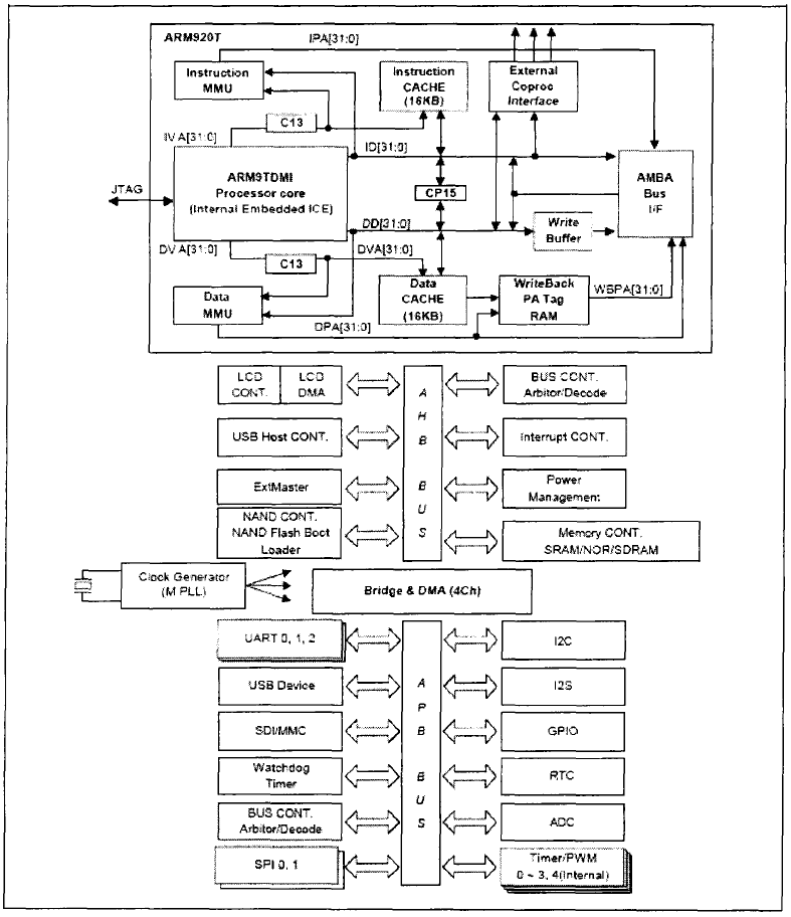

Figure 3. S3C2410 internal structure diagram.

Hardware platform based on S3C2410

The hardware platform in this paper has integrated 64MB SDRAM, 64 MBNANDFLASH storage devices, and also provided rich peripheral interfaces: CS89OO Ethernet card interface, 2 UART communicating with PC, one LCD interface, USB master-slave port and so on. The structure of embedded hardware platform is as shown in Figure 4.

Of which the serial port and 10M internet access are the main auxiliary ports of subsequent debugging work. The USB interface has master-slave ports, the primary interface can connect USB device directly; from the connection of interface and personal computer, the development board is as the slave device, and the PC file can be quickly downloaded to the development board.

THE TEST RESULT OF HARDWARE SYSTEM

The testing environment. The testing environment of system is the designed system hardware module interconnecting with PC through network, constituting a simple internal LAN. Through the internet sniffer, the data traffic of internet can be statistic, and instantaneity of system can be analyzed through the DSP/BIOS tools of CCS.

Performance parameter. After the test, the main performance parameters of this system are shown in Table 1.Through the observation of the parameters, it can be concluded that the hardware system has accomplished the purpose of original design.

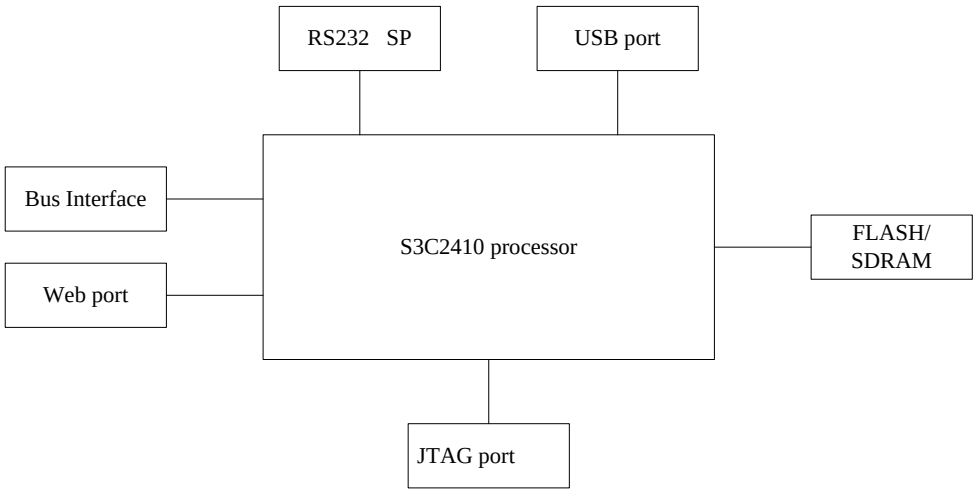

Figure 4. The architecture of ARM hardware platform.

Table 1. The performance parameter.

Image compression format	**H.264**
Image resolution	Cif (352*288)
Maximum coding speed	15 fps
Data traffic	50-200 kbps
The mean of data flow	About 80 kbps
Networking protocol	Ip/udp/rtp
Network interface	Rj-45 100 mbps

CONCLUSION

This paper, combined with the advantages of ARM and DSP, has proposed embedded image processing system based on ARM and DSP, solving the faults of low processing efficiency and small amount of calculation of traditional single processor system. From the performance parameters of the test, it can be concluded that the designed system in this paper achieves cooperative work on the ARM and DSP hardware platform, realizing the data real-time transmission, and it has an important guiding significance for the improvement of image processing system. Meanwhile, it has played a positive role on the realization of engineering application and social significance brought by engineering application in the field of signal processing areas which requiring large computation, complex dispose, strong data throughput.

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